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**Abstract**

The goal of this project is to gain experience in VLSI design by designing a chip that will process digital streaming audio data. More specifically, we will implement a 512-tap digital finite impulse response (FIR) filter, which will be applied to an input stream in order to create an output stream. We used the I2C protocol to allow a host to control the chip and the serial I2S protocol for transferring digital audio streams in and out.

Our hardware design was represented using Verilog register-transfer level (RTL) code. Development has been done using Xilinx ISE Design Suite 14.7. Test-benches were also designed and implemented using Verilog. The end goal of the project is to implement the design on a field-programmable gate array (FPGA). We will bring up our FPGA design with a realistic environment including an audio source, audio sink, and a microcontroller for reading and writing registers. We also plan to send a simple CMOS integrated circuit design for fabrication by MOSIS that will help us gain experience in physical chip design and prepare future groups to fabricate our full design.

**Keywords:** Application-specific integrated circuit (ASIC), Very large scale integration (VLSI) I2S, I2C, Digital filtering